WHAT IS CLAIMED IS:

1. An automatic gain control (AGC) apparatus comprising:

an analog variable gain amplifier;

a digital variable gain amplifier coupled to an output of the analog variable gain amplifier; and

a gain controller adapted to measure a signal output from the digital variable gain amplifier and to control the gains of the analog and digital variable gain amplifiers.

2. The apparatus of claim 1, further comprising:

a DC offset canceller interposed between the output of the analog variable gain amplifier and an input of the digital variable gain amplifier, wherein an AGC loop gain is varied according to an operating mode of the DC offset canceller.

3. A method of operating an automatic gain control (AGC) loop in combination with a DC loop, comprising:

selecting a particular DC operating mode for the DC loop from among a plurality of possible DC operating modes;

operating the DC loop in the selected DC operating mode to correct for DC offset in a desired signal;

selecting a particular AGC operating mode for the AGC loop from among a plurality of possible AGC operating modes based on the selected DC operating mode; and

operating the AGC loop in the selected AGC operating mode to provide variable gain for the desired signal.

4. The method of claim 3, wherein the plurality of possible DC operating modes include an acquisition mode and a tracking mode.

5. The method of claim 4, wherein the acquisition mode has a wider loop bandwidth than that of the tracking mode and is used to more quickly remove a large DC offset in the desired signal.

6. The method of claim 3, wherein each of the plurality of possible AGC operating modes is associated with a respective AGC loop gain.

7. The method of claim 3, wherein the plurality of possible AGC operating modes includes a normal mode and a low gain mode.

8. The method of claim 7, wherein the plurality of possible AGC operating modes further include a freeze mode.

9. The method of claim 4, wherein the selected AGC operating mode is a low gain mode when the selected DC operating mode is the acquisition mode.

10. The method of claim 4, wherein the selected AGC operating mode is a freeze mode when the selected DC operating mode is the acquisition mode.

11. A receiver unit in a wireless communication system, comprising:

a DC loop configurable to operate in one of a plurality of possible DC operating modes to correct for DC offset in a desired signal; and

an automatic gain control (AGC) loop configurable to operate in one of a plurality of possible AGC operating modes to provide variable gain for the desired signal, wherein the particular AGC operating mode to be used is determined based on the particular DC operating mode selected for use for the DC loop.

12. An control apparatus in a wireless communication system, comprising:

means for selecting a particular DC operating mode for a DC loop from among a plurality of possible DC operating modes;

means for operating the DC loop in the selected DC operating mode to correct for DC offset in a desired signal;

means for selecting a particular AGC operating mode for an automatic gain control (AGC) loop from among a plurality of possible AGC operating modes based on the selected DC operating mode; and

means for operating the AGC loop in the selected AGC operating mode to provide variable gain for the desired signal.

13. A method of operating a DC loop in a receiver unit, comprising:

selecting a particular operating mode for the DC loop from among a plurality of possible operating modes that include an acquisition mode; and

if the selected operating mode is the acquisition mode,

operating the DC loop in the acquisition mode for a particular time duration to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

transitioning out of the acquisition mode after the particular time duration.

14. The method of claim 13, wherein the acquisition mode is selected in response to an event expected to result in a large DC offset in the desired signal.

15. The method of claim 14, wherein the event corresponds to a switch to new analog circuit stages to process the desired signal.

16. The method of claim 14, wherein the event corresponds to application of a new DC offset value to correct for static DC offset in the desired signal.

17. The method of claim 13, wherein the plurality of possible operating modes further include a tracking mode.

18. The method of claim 17, wherein the transition is made from the acquisition mode to the tracking mode after the particular time duration.

19. The method of claim 13, wherein the particular time duration is further selected based on an expected amplitude of the DC offset in the desired signal.

20. The method of claim 13, wherein the particular time duration is further selected to minimize a combination of DC offset introduced in the desired signal and loop noise from the DC loop.

21. A DC loop in a receiver unit, comprising:

a summer operative to subtract a DC offset value from a desired signal to provide a DC offset corrected signal; and

a loop control unit configurable to operate in one of a plurality of possible operating modes to provide the DC offset value, wherein the plurality of possible operating modes include an acquisition mode having a particular loop bandwidth, and wherein the loop control unit is operated in the acquisition mode, when selected, for a particular time duration inversely proportional to the loop bandwidth for the acquisition mode and to transition out of the acquisition mode after the particular time duration.

22. An apparatus in a receiver unit, comprising:

means for selecting a particular operating mode for a DC loop from among a plurality of possible operating modes that include an acquisition mode; and

means for operating the DC loop in the acquisition mode for a particular time duration, if the selected operating mode is the acquisition mode, to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

means for transitioning out of the acquisition mode after the particular time duration.

23. A method of digitally amplifying a desired signal, comprising:

receiving a gain represented in a logarithm format;

determining a difference between the received gain and a gain offset;

converting the difference, represented in the logarithm format, to an output gain represented in a linear format; and

digitally multiplying the desired signal with the output gain.

24. A digital variable gain amplifier (DVGA) comprising:

a first unit operative to receive a gain represented in a logarithm format and to determine a difference between the received gain and a gain offset;

a second unit operative to convert the difference, represented in the logarithm format, to an output gain represented in a linear format; and

a digital multiplier operative to multiply input samples with the output gain to provide output data.

25. The DVGA of claim 24, further comprising:

a multiplexer operative to multiplex inphase and quadrature input samples into a single sequence of samples, and wherein the digital multiplier is operative to multiply the inphase and quadrature input samples in a time-division multiplexed manner.

26. An apparatus for digitally amplifying a desired signal, comprising:

means for receiving a gain represented in a logarithm format;

means for determining a difference between the received gain and a gain offset;

means for converting the difference, represented in the logarithm format, to an output gain represented in a linear format; and

means for digitally multiplying the desired signal with the output gain.

27. A method of controlling one or more analog circuits via a serial bus, comprising:

receiving a control for a particular analog circuit;

forming a message corresponding to the received control;

sending the message over the serial bus;

receiving the message at the particular analog circuit; and

adjusting one or more characteristics of the particular analog circuit based on the received message.

28. The method of claim 27, wherein the particular analog circuit is an amplifier configurable to operate at one of a plurality of discrete gains, and wherein the message is indicative of a specific discrete gain to be used for the amplifier.

29. The method of claim 27, wherein the message is used to adjust a bias current for the particular analog circuit.

30. The method of claim 27, wherein the message is used to adjust the frequency for a signal generated by the particular analog circuit.

31. The method of claim 27, wherein each of the one or more analog circuits is assigned a respective priority, and wherein messages are sent to the one or more analog circuits based in part on their assigned priorities.

32. The method of claim 27, wherein each of the one or more analog circuits is associated with a respective address.

33. An apparatus for controlling one or more analog circuits via a serial bus, comprising:

means for receiving a control for a particular analog circuit;

means for forming a message corresponding to the received control;

means for sending the message over the serial bus;

means for receiving the message at the particular analog circuit; and

means for adjusting one or more characteristics of the particular analog circuit based on the received message.

34. A receiver unit comprising:

an RF front-end unit operative to amplify, downconvert, and digitize a received signal to provide samples;

a digital signal processor operative to process the samples to provide output data; and

a serial bus interface (SBI) unit operative to provide controls for the RF front-end unit via a serial bus.

35. The receiver unit of claim 34, wherein the SBI unit is configured to support a plurality of hardware request channels.

36. The receiver unit of claim 35, wherein each hardware request channel is associated with a respective priority.

37. The receiver unit of claim 35, wherein each hardware request channel is operable to send messages via a plurality of possible data transfer modes.

38. The receiver unit of claim 37, wherein the plurality of possible data transfer modes include a fast transfer mode and an interrupt transfer mode.

39. A method of processing a desired signal in a wireless communication system, comprising:

amplifying the desired signal with a first gain having a coarse resolution;

downconverting the amplified signal from radio frequency (RF) to baseband with a single frequency downconversion stage;

digitizing the downconverted signal to provide samples; and

digitally amplifying the samples with a second gain having a fine resolution to provide output data having a desired signal amplitude.

40. The method of claim 39, further comprising:

correcting for DC offset in the samples with a DC loop, wherein the DC offset corrected samples are digitally amplified.

41. A direct downconversion receiver comprising:

an RF front-end unit operative to amplify, downconvert, and digitize a received signal to provide samples;

a digital variable gain amplifier (DVGA) operative to amplify the samples with a first gain to provide output data having a desired signal amplitude; and

an automatic gain control (AGC) loop operative to provide the first gain for the DVGA based in part on the output data.

42. The direct downconversion receiver of claim 40, further comprising:

a DC offset canceller operative to correct for DC offset in the samples, and wherein the DVGA is operative to amplify the DC offset corrected samples.

43. The direct downconversion receiver of claim 40, wherein the AGC loop is further operative to provide a second gain for the RF front-end unit.

44. An apparatus in a wireless communication system, comprising:

first means for amplifying a received signal;

means for canceling a DC offset in the amplified signal;

second means for digitally amplifying the DC offset cancelled signal; and

means for measuring the digitally amplified signal and to control the gains of the first and second amplifying means.

45. A receiver unit comprising:

an analog variable gain amplifier;

a DC offset canceller coupled to an output of the analog variable gain amplifier;

a digital variable gain amplifier coupled to an output of the DC offset canceller;

a gain controller adapted to measure a signal output from the digital variable gain amplifier and to control the gains of the analog and digital variable gain amplifiers; and

a serial bus interface (SBI) unit operative to provide the gain for the analog variable gain amplifier via a serial bus.

46. A receiver unit comprising:

an RF front-end unit operative to amplify, downconvert, and digitize a received signal to provide samples;

a DC loop operative to cancel DC offset in the samples;

a digital variable gain amplifier (DVGA) operative to amplify the DC offset canceled samples with a first gain to provide output data having a desired signal amplitude;

an automatic gain control (AGC) loop operative to provide the first gain for the DVGA and a second gain for the RF front-end unit based in part on the output data; and

a serial bus interface (SBI) unit operative to provide the second gain to the RF front-end unit.